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Title: PLANARIZED SEMICONDUCTOR INTERCONNECT TOPOGRAPHY AND METHOD FOR POLISHING A METAL LAYER TO FORM INTERCONNECT

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Derrick Brown

PRELIMINARY AMENDMENT

Commissioner for Patents
Washington, D.C. 20231

Dear Sir/Madam:

The captioned application is a continuation application pursuant to 37 C.F.R. § 1.53(b) from prior application 09/143,723 filed August 31, 1998. Prior to initial examination of the captioned matter, please amend the case as follows:

In the Specification:

Please amend the specification as follows. A "marked-up" version of these amendments is included in **Attachment A**.

Please replace the paragraph on pg. 4, line 13 - pg. 5, line 3 with the following:

Unfortunately, the topological surface of the interconnect level is not absent of elevational disparity. That is, the upper surface of interconnect 38 includes a recessed area 42 that extends below a substantially planar upper surface 44 of interlevel dielectric 20. Recessed area 42 may result from a phenomena known as the "dishing" effect. Dishing naturally results

from the polishing pad flexing or conforming to the surface being polished. If the surface being polished is initially bowed or arcuate (i.e., is not planar), the polishing pad will take on the shape of the non-planar regions causing further dishing of the surface being polished. The CMP slurry initiates the polishing process by chemically reacting with the surface material in both elevated and recessed areas. Because of the deformation of the CMP pad, the reacted surface material in recessed areas may be physically stripped in addition to the reacted surface material in elevated areas. As such, a surface having fluctuations in elevation may continue to have some elevational disparity even after it has been subjected to CMP. The dishing effect is particularly a problem when forming a relatively wide interconnect between regions of a dielectric that is substantially more dense than the metal. While the dielectric is hard enough to support the overlying regions of the CMP pad, the metal is not, and thus allows significant flexing of the pad. Such flexing of the CMP pad causes the surface of the metal interconnect to become recessed relative to adjacent regions of the dielectric.

Please replace the paragraph on pg. 5, line 19 - pg. 6, line 4 with the following:

It would therefore be desirable to develop a polishing process which can achieve global planarization across the entire topological surface of an interconnect level. Global planarization requires that the polish rate be uniform in all elevated areas of the topography. Such uniformity of the polish rate is particularly needed when polishing a topography having a set of interconnect which is of relatively narrow lateral dimension spaced from a relatively wide interconnect. Herein, narrow and wide refer to a lateral dimension which extends along the trench base perpendicular and co-planar with the elongated axis of the interconnect. That is, the dielectric in the space between the series of narrow interconnect and the wide interconnect needs to be polished as quickly as the interconnect are polished in order to assure both densely spaced narrow interconnects and sparsely spaced wide interconnects have a flat and relatively co-planar upper surface. The desirous polishing process must avoid problems typically arising during CMP, for example, metal dishing or oxide erosion.

Please replace the paragraph on pg. 13, line 15 - pg. 14, line 2 with the following:

A plurality of dummy trenches 56 may be formed in dielectric layer 50 between a series of relatively narrow trenches 52 and a relatively wide trench 54. While the dimensions of these trenches may vary depending on the design specifications, the dummy trenches 56 are preferably 1 to 5 microns in width, the narrow trenches 52 preferably have sub-micron widths, and the wide trench 54 is preferably greater than 50 microns in width. Also, the depths of all the trenches may range from 2,000 Å to 1 micron. Further, the set of relatively narrow trenches 52 may be spaced apart by a distance of less than 1 micron and from the relatively wide trench 54 by a distance greater than 50 microns. Although the spacing between dummy trenches 56 may vary, this spacing may, e.g., range from 0.5 micron to 50 micron. The trenches may be formed by lithographically patterning a photoresist layer upon dielectric layer 50 to expose select portions of the depicted dielectric. The select portion of dielectric layer 50 not covered by the patterned photoresist is then etched using an etch technique, e.g., a CF_4 plasma etch.

<u>In the Claims:</u>

Please amend claims 1, 9, and 17 to read as follows. A "marked-up" version of these amendments is included in **Attachment A**.

1. (Amended) A method, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches;

filling said trenches with a conductive material;

polishing said conductive material to form dummy conductors in said dummy trenches and interconnect in said narrow and wide trenches, wherein said dummy conductors are electrically separate from of electrically conductive features of an ensuing integrated circuit.

9. (Amended) A method, comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a trench which is to receive a relatively wide interconnect feature and a series of trenches which are to receive relatively narrow interconnect features;

filling said plurality of dummy trenches with a conductive material; and

polishing said conductive material to form dummy conductors, wherein said dummy conductors are electrically separate from electrically conductive features of an ensuing integrated circuit.

17. (Amended) A substantially planar semiconductor topography, comprising:

a plurality of laterally spaced dummy trenches in a dielectric layer, between a relatively wide trench and a series of relatively narrow trenches;

dummy conductors in said dummy trenches and electrically separate from electrically conductive features below said dummy conductors; and

conductive lines in said narrow and wide trenches, wherein upper surfaces of said conductive lines are substantially coplanar with dummy conductor upper surfaces.

Please add the following claims

21. (Added) The method of claim 1, wherein said dummy conductors are substantially co-planar with said interconnect.

22. (Added) The method of claim 9, wherein said dummy conductors are substantially co-planar with said interconnect.

CONCLUSION

In the present Amendment, the Specification and claims 1, 9, and 17 have been amended; claims 21 and 22 have been added. Therefore, pending claims 1-22 are presented for consideration by the Examiner. If the Examiner has any questions, comments, or suggestions, the undersigned earnestly requests a telephone conference.

Respectfully submitted,

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Date: February 7, 2001

ATTACHMENT A

"Marked-up" amendments as follows:

In the Specification:

Page 4, line 25, after the phrase "when forming" please delete "an" and substitute therefor --a--.

Page 5, line 26, after the phrase "wide interconnect needs" please insert --to--.

Page 13, lines 23-24, after the phrase "from 0.5 micron to 50 micron" please delete the following text: **[Gentlemen, are the dimensions and spacings listed here for the trenches correct?]**.

In the Claims:

1. (Amended) A method [for providing a substantially planar semiconductor topography which extends above a plurality of electrically conductive features that form an integrated circuit], comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a relatively wide trench and a series of relatively narrow trenches;

filling said [dummy trenches and said wide and narrow] trenches with a conductive material;

polishing said conductive material to form dummy conductors [exclusively] in said dummy trenches and interconnect [exclusively] in said narrow and wide trenches, wherein said dummy conductors are electrically separate from [said plurality of] electrically conductive features [and co-planar with said interconnect] of an ensuing integrated circuit.

9. (Amended) A method [for providing a semiconductor topography having a plurality of electrically conductive features and a topography which is substantially planar], comprising:

etching a plurality of laterally spaced dummy trenches into a dielectric layer between a trench which is to receive a relatively wide interconnect feature and a series of trenches which are to receive [a] relatively narrow interconnect [feature] features;

filling said plurality of dummy trenches with a conductive material; and

polishing said conductive material to form dummy conductors [bounded exclusively within], wherein said dummy [trenches] conductors are electrically separate from [said] electrically conductive features[, and such that first upper surfaces of said dummy conductors are substantially co-planar with second upper surfaces of said relatively wide and narrow interconnect features] of an ensuing integrated circuit.

17. (Amended) A substantially planar semiconductor topography [elevationally raised above a plurality of electrically conductive features which receive electrically transitory voltages forwarded through an integrated circuit], comprising:

a plurality of laterally spaced dummy trenches [residing within] in a dielectric layer, between a relatively wide trench and a series of relatively narrow trenches;

dummy conductors [bounded exclusively within] in said dummy trenches and electrically separate from [said plurality of] electrically conductive features below said dummy conductors; and

[interconnect bounded exclusively within] conductive lines in said narrow and wide trenches, wherein [interconnect] upper surfaces of said conductive lines are substantially coplanar with dummy conductor upper surfaces.

21. (Added) The method of claim 1, wherein said dummy conductors are substantially co-planar with said interconnect.

22. (Added) The method of claim 9, wherein said dummy conductors are substantially co-planar with said interconnect.